What is claimed is:

1. A semiconductor device for use in a memory cell, comprising:

an active matrix provided with a semiconductor substrate, a transistor formed on the semiconductor substrate, an isolation region for isolating the transistor and a first insulating layer formed on top of the transistor and the isolation region;

a capacitor structure, formed on top of the first insulating layer, composed of a bottom electrode, a capacitor thin film placed on top of the bottom electrode and a top electrode formed on top of the capacitor thin film;

a second insulating layer formed on top of the transistor and the capacitor structure;

a metal interconnection formed on top of the second insulating layer to electrically connect the transistor to the capacitor structure;

a barrier layer formed on top of the metal interconnection; and

an inter-metal dielectric (IMD) layer formed on top of the barrier layer by using a plasma chemical vapor deposition (CVD) in a hydrogen rich atmosphere, wherein the barrier layer is used for preventing the capacitor structure from the hydrogen.

2. The semiconductor device of claim 1, wherein the

capacitor thin film is made of a ferroelectric material selected from a group consisting of SBT (SrBiTaOx), PZT (PbZrTiOx) or the like.

3. The semiconductor device of claim 2, wherein the IMD layer is made of a oxide material such as SiO_2.

4. The semiconductor device of claim 3, wherein the plasma CVD is carried out at a low temperature by using silane (SiH_4) as a source gas.

5. The semiconductor device of claim 1, wherein the barrier layer is made of a material such as Al_2O_3.

6. The semiconductor device of claim 5, wherein the barrier layer has a thickness ranging from approximately 50 Å to approximately 150 Å.

7. The semiconductor device of claim 6, wherein the barrier layer is formed by using an atomic layer deposition (ALD) method.

8. The semiconductor device of claim 7, wherein the ALD method is carried out by using trimethyl aluminum (TMA) and H_2O as a source gas and using N_2 as a purge gas.

9. The semiconductor device of claim 1, further

comprising:

a metal line formed on top of the IMD layer;

an additional barrier layer formed on top of the metal line;

a passivation layer formed on top of the additional barrier layer by using a plasma CVD in a hydrogen rich atmosphere, wherein the additional barrier layer is used for preventing the capacitor structure from the hydrogen.

10. The semiconductor device of claim 9, wherein the additional barrier layer is made of a material such as Al_2O_3.

11. The semiconductor device of claim 10, wherein the additional barrier layer is formed by using an ALD method.

12. A method for manufacturing a semiconductor device for use in a memory cell, the method comprising the steps of:

a) preparing an active matrix provided with a transistor and a first insulating layer formed around the transistor;

b) forming a capacitor structure on top of the first insulating layer, wherein the capacitor structure includes a capacitor thin film made of a ferroelectric material;

c) forming a first metal layer and patterning a first metal layer into a first predetermined configuration to electrically connect the transistor to the capacitor structure;

d) forming a first barrier layer on top of the patterned

first metal layer; and

e) forming an inter-metal dielectric (IMD) layer formed on top of the first barrier layer by using a plasma chemical vapor deposition (CVD) in a hydrogen rich atmosphere, wherein the barrier layer is used for preventing the capacitor structure from the hydrogen.

13. The method of claim 12, wherein the capacitor thin film is made of a material selected from a group consisting of SBT, PZT or the like.

14. The method of claim 13, wherein the IMD layer is made of a oxide material such as SiO_2.

15. The method of claim 14, wherein the plasma CVD is carried out at a low temperature by using SiH_4 as a source gas.

16. The method of claim 15, wherein the first barrier layer is made of a material such as Al_2O_3.

17. The method of claim 16, wherein the first barrier layer has a thickness ranging from approximately 50 Å to approximately 150 Å.

18. The method of claim 17, wherein the first barrier layer is formed by using an ALD method.

19. The method of claim 18, wherein the ALD method is carried out by using TMA and H_2O as a source gas and using N_2 as a purge gas.

20. The method of claim 12, after the step e), further comprising the steps of:

f) a second metal layer formed on top of the IMD layer;

g) a second barrier layer formed on top of the second metal layer; and

h) a passivation layer formed on top of the additional barrier layer by using a plasma CVD in a hydrogen rich atmosphere, wherein the additional barrier layer is used for preventing the capacitor structure from the hydrogen.

21. The method of claim 20, wherein the second barrier layer is made of a material such as Al_2O_3.

22. The semiconductor device of claim 21, wherein the step g) is carried out by using an ALD method.